Features

- ESD Protect for Super Speed Differential Signaling (above 5Gb/s) channels
- Protects six I/O lines and one V_{DD} line
- Provide ESD protection for each channel to **IEC 61000-4-2, (ESD) ±15kV (air), ±8kV (contact)**
- **For 5V and below 5V operating voltage**
- **Ultra low capacitance: 0.35pF max.**
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Back-drive protection for power-down mode
- ***Green part***

Applications

- **USB3.0**
- **HDMI 1.4**
- **High Speed I/O Ports in Any Electronic Product**

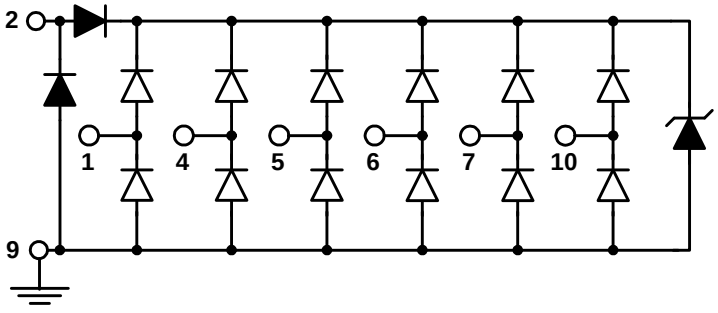
Description

AZ1065-06F is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1065-06F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

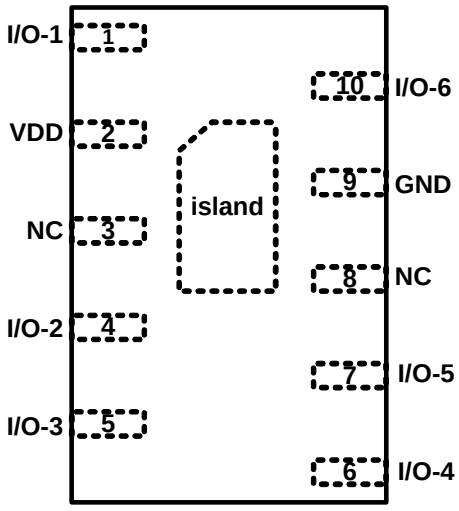
AZ1065-06F is a unique design which includes surge rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components. Besides, there is a back-drive protection design in AZ1065-06F for power-down mode operation.

AZ1065-06F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



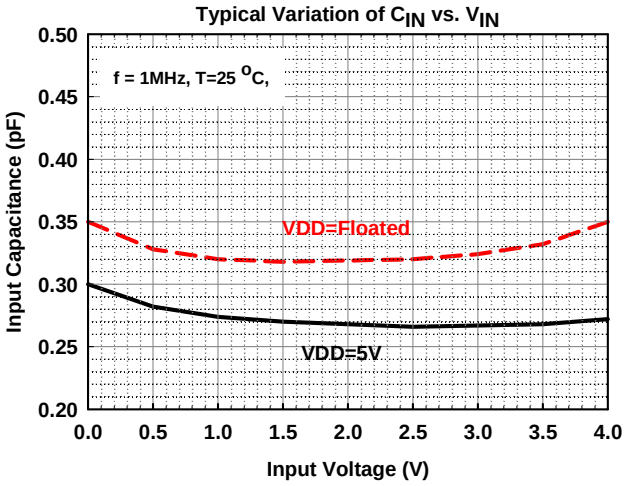
DFN4120P10E
(Top View)

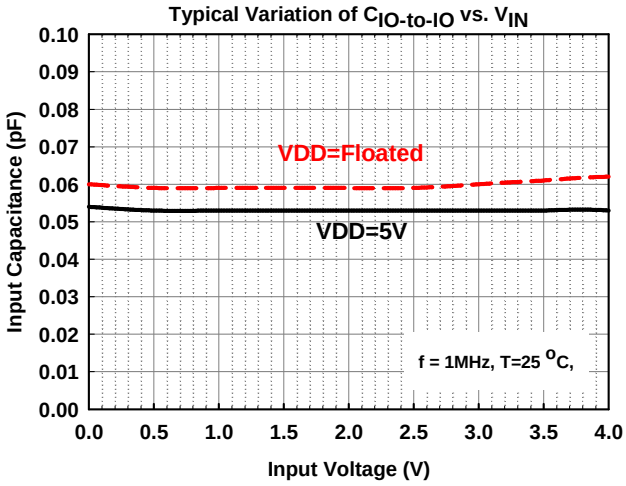
SPECIFICATIONS

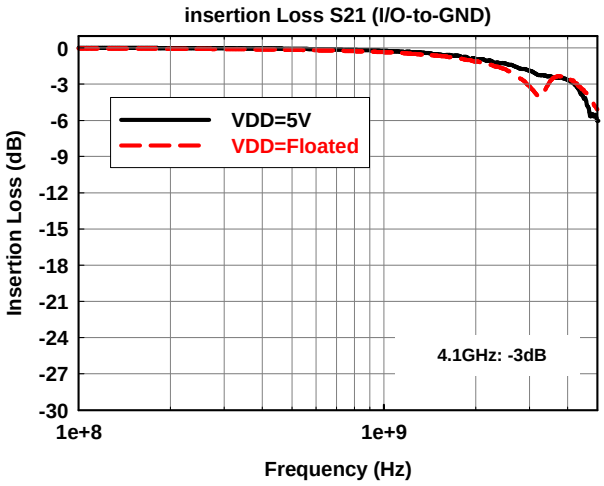
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Operating Supply Voltage (VDD-GND)	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ±8	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-40 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

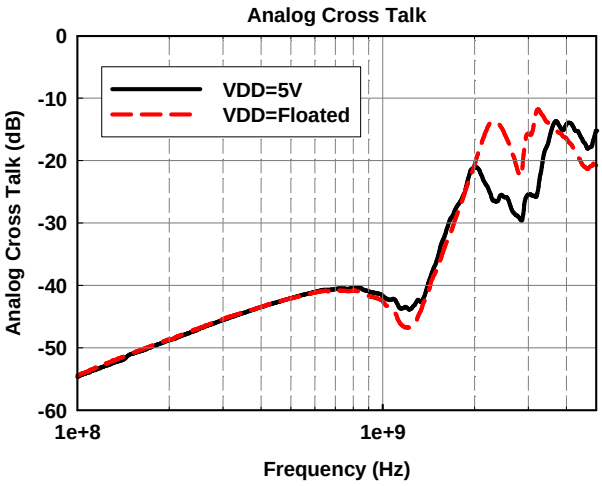
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 2 to pin 9, T=25 °C.			5	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, Pin 2 to pin 9.			2.5	**μA**
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin\ 2}$ = 5V, $V_{Pin\ 9}$ = 0V, T=25 °C.			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Pin 2 to Pin 9.	6		9.5	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, Pin 9 to Pin 2.		0.8	1.2	**V**
ESD Clamping Voltage –I/O	V_{clamp_io}	IEC 61000-4-2 +6kV,T=25 °C,Contact mode, Any Channel pin to Ground.		13		**V**
ESD Clamping Voltage –VDD	V_{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground.		10		**V**
ESD Dynamic Turn-on Resistance –I/O	$R_{dynamic\_io}$	IEC 61000-4-2, 0~+6kV,T=25 °C, Contact mode, Any Channel pin to Ground.		0.35		**Ω**
ESD Dynamic Turn-on Resistance –VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2, 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground.		0.2		**Ω**
Channel Input Capacitance	C_{IN}	**V_{pin2} = 5V,** V_{pin9} = 0V,**V_{IN} = 2.5V**,f = 1MHz, T=25 °C, Any Channel pin to Ground.		0.27	0.35	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	**V_{pin2} = 5V,** V_{pin9} = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C , Between Channel pins.		0.05	0.07	**pF**

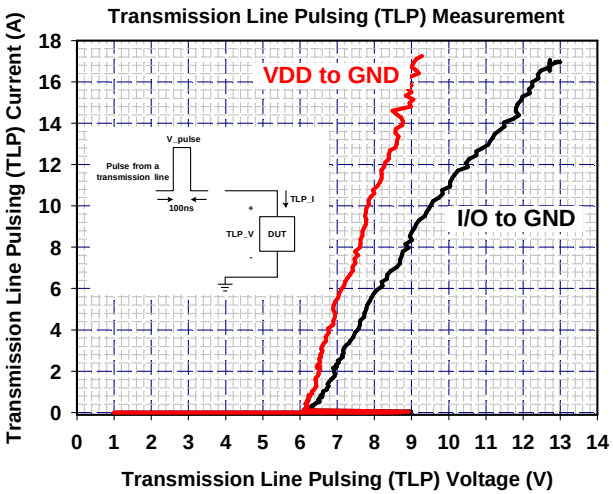
Typical Characteristics











Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. The diode D3 is a back-drive protection design, which blocks the DC back-drive current when the potential of I/O pin is greater than that of VDD pin. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + Breakdown voltage drop of D3 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZ1065-06F has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

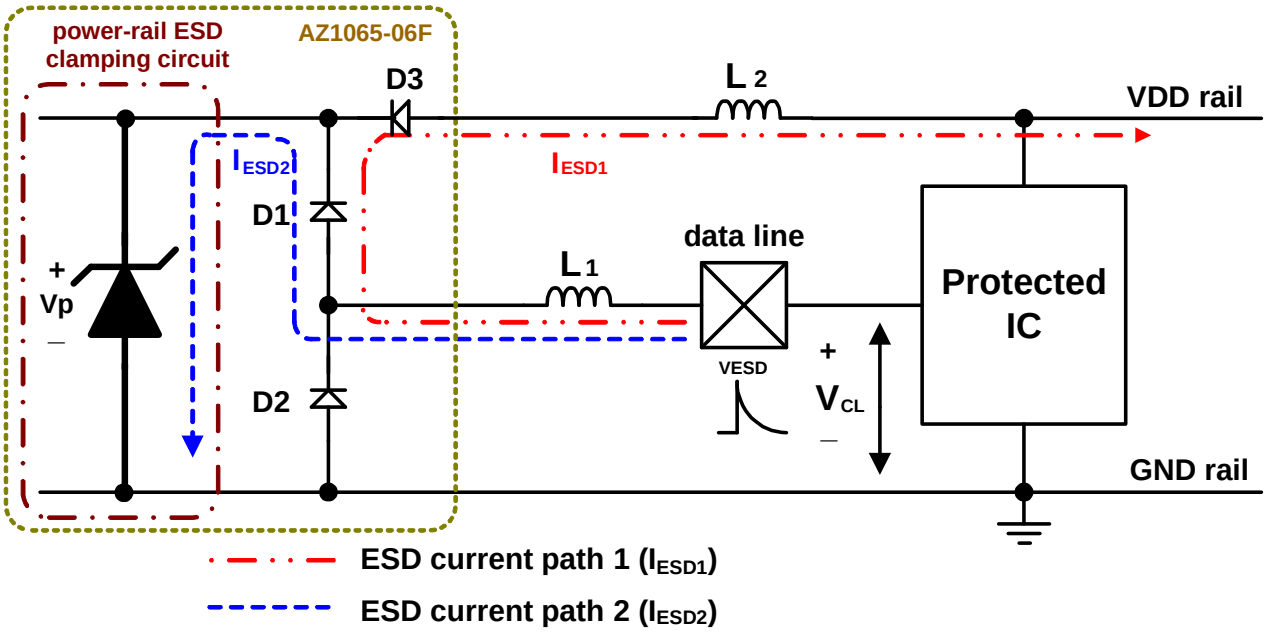


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZ1065-06F is designed to protect six data lines and one power rail from transient over-voltage (such as ESD stress pulse). The device connection of AZ1065-06F is shown in the Fig. 2. In Fig. 2, the six protected data lines are connected to the ESD protection pins (pin1, pin4, pin5, pin6, pin7, and pin10) of AZ1065-06F. The ground pin (pin9) of AZ1065-06F is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 2) of AZ1065-06F is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ1065-06F.

AZ1065-06F can provide protection for 6 I/O signal lines simultaneously. If the number of I/O signal lines is less than 6, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ1065-06F.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 2) of AZ1065-06F can be left as floating. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

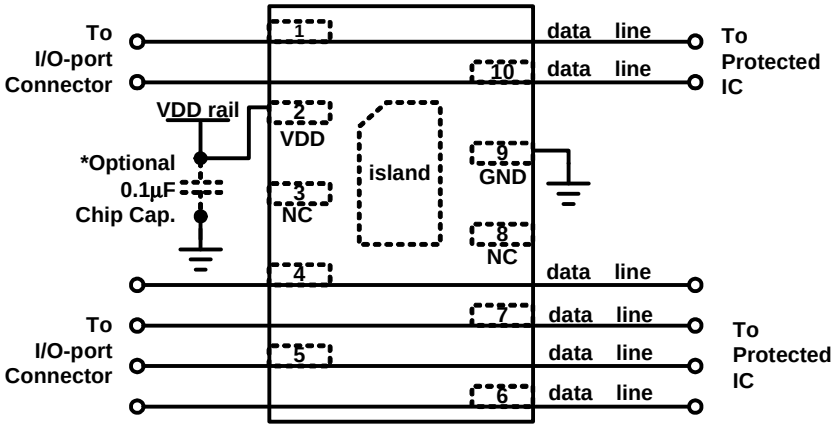


Fig. 2 Data lines and power rails connection of AZ1065-06F.

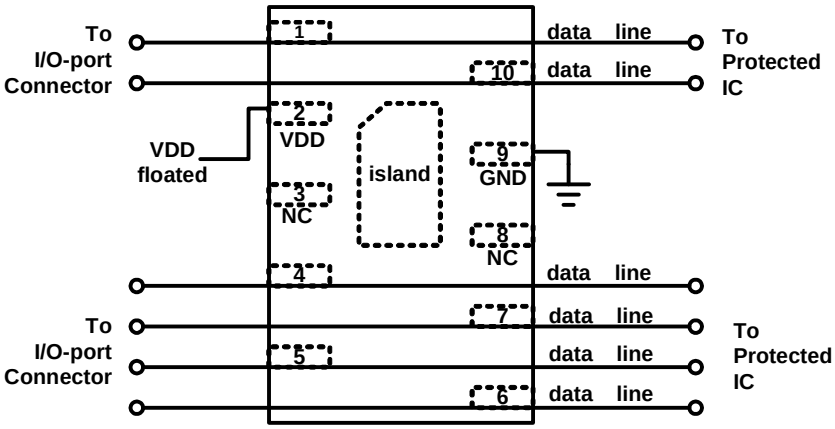


Fig. 3 Data lines and power rails connection of AZ1065-06F. VDD pin is left as floating when no power rail presented on the PCB.

C. Application

AZ1065-06F is designed for protecting high speed I/O ports from over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZ1065-06F, especially, the USB3.0 port.

USB3.0 Protection for Super Speed Differential signals

USB3.0 is expected to transmit and receive above 5Gb/s data, which needs differential signaling. For differential signaling, keep the differential impedance at constant is the most importance.

ESD protection devices have an inherent junction capacitance. Usually, this added capacitance on an USB3.0 port will cause the impedance of the differential pair to drop to interfere with the signaling. The AZ1065-06F presents only **0.35pF** max. capacitance to each differential signal while being rated to handle 8kV ESD contact/air discharges as outlined in IEC 61000-4-2 and providing a low clamping voltage to protect the downstream devices.

Therefore, AZ1065-06F is the most suitable ESD protector for USB3.0 I/O port and other high speed, above 5Gb/s, I/O ports in any electronic product. Fig.4 shows the PCB layout example for USB3.0 I/O port. Fig. 5 shows the 5GHz Eye Diagram when the AZ1065-06F is used. No degradation is observed.

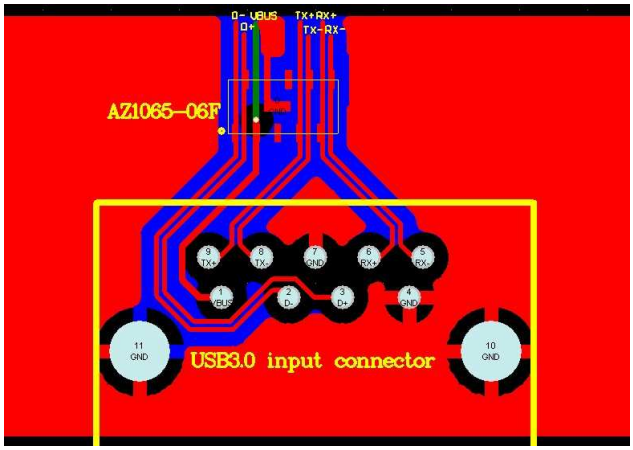


Fig. 4 USB3.0 ESD Protection by using AZ1065-06F.

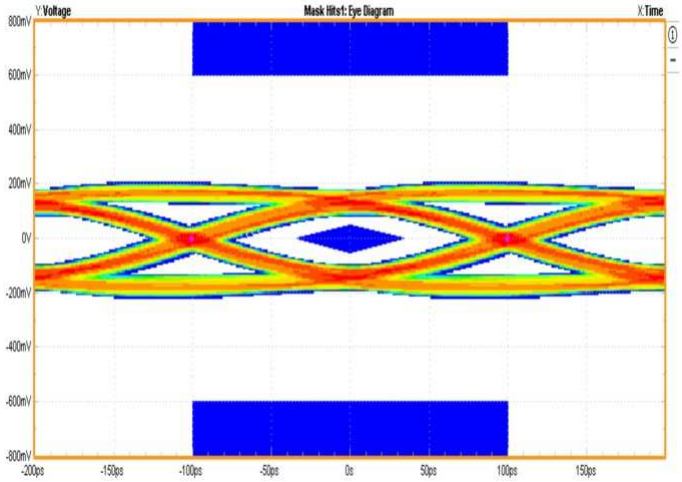
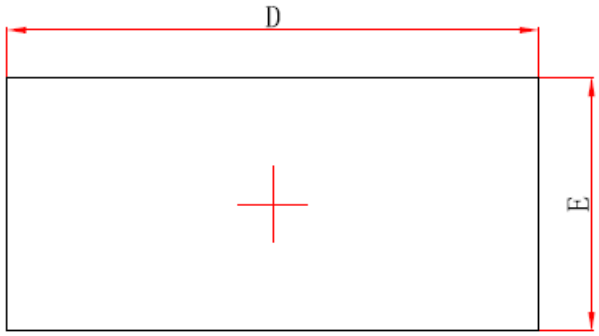


Fig. 5 The 5GHz Eye Diagram when AZ1065-06F is used.

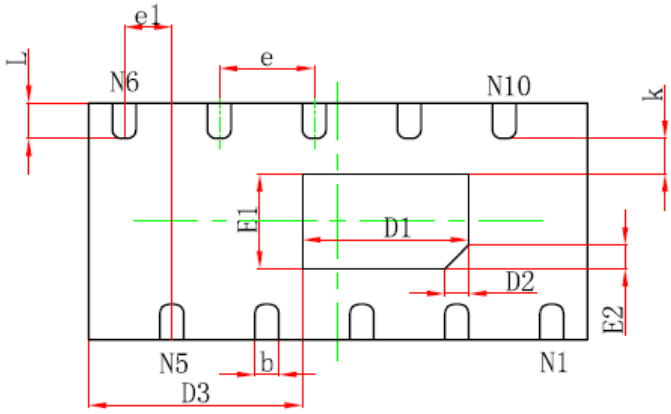
Mechanical Details

DFN4120P10E

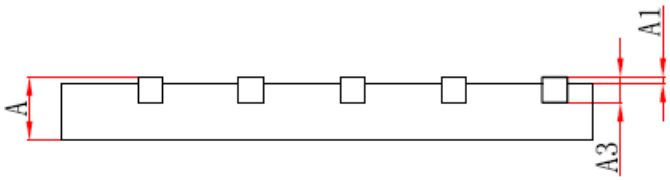
PACKAGE DIAGRAMS AND DIMENSIONS



Top View



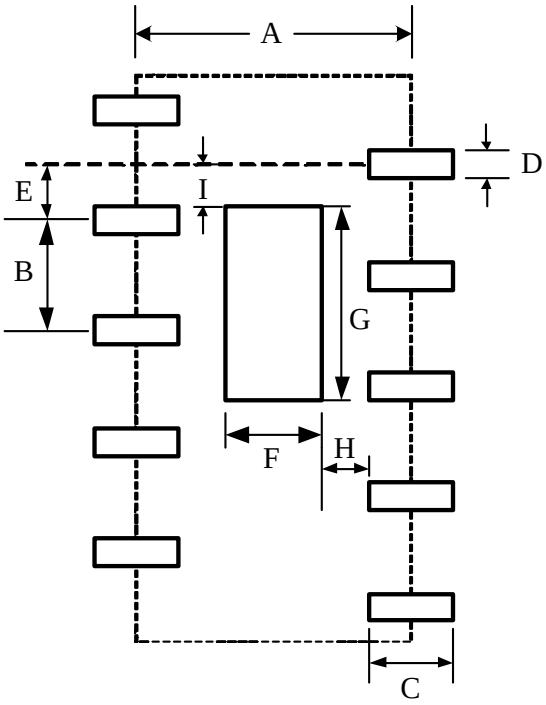
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.152 REF		0.006REF	
D	4.050	4.150	0.159	0.163
E	1.950	2.050	0.077	0.081
D1	1.300	1.500	0.051	0.059
E1	0.700	0.900	0.028	0.035
D3	1.650	1.850	0.065	0.073
D2	0.200REF		0.008REF	
E2	0.200REF		0.008REF	
k	0.200MIN		0.008MIN	
b	0.150	0.250	0.006	0.010
e	0.800TYP		0.031TYP	
e1	0.350	0.450	0.014	0.018
L	0.250	0.350	0.010	0.014

LAND LAYOUT

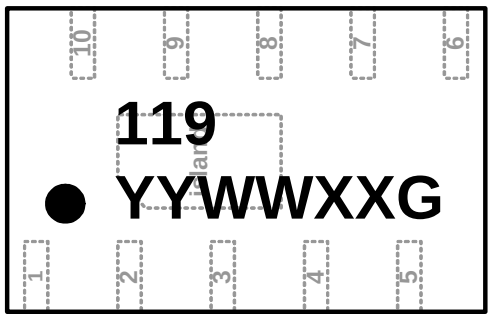


Symbol	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.924	2.000	2.076	0.076	0.079	0.082
B	0.800TYP.			0.031TYP.		
C	0.600TYP.			0.023TYP.		
D	0.150	0.200	0.250	0.006	0.008	0.010
E	0.400TYP.			0.015TYP.		
F	0.700	0.800	0.900	0.028	0.031	0.035
G	1.300	1.400	1.500	0.051	0.055	0.059
H	0.200MIN.			0.008MIN.		
I	0.300TYP.			0.012TYP.		

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
AZ1065-06F	119

119 = Device Code
YYWW = Date Code
XX = Control Code
G = Green part

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ1065-06F.R7G	Green	T/R	7 inch	3 reel= 9,000/box	6 box =54,000/carton

Revision History

Revision	Modification Description
Revision 2010/01/19	Formal Release.
Revision 2010/08/19	Add and modify the parameters of D3, D2, E2, e, and e1 in PACKAGE DIAGRAMS AND DIMENSIONS
Revision 2011/05/15	1. Update the Company Logo. 2. Add the Ordering Information.
Revision 2012/05/11	Add the typical dimensions of A, D, F, G, and I in LAND LAYOUT.
Revision 2012/07/11	Add the max. value for V_{BV}.